DJH
10-3-06

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	67	pipeline near2 accelerat$3	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/03 13:48
L3	3	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/03 13:49
S1	86	pipeline near2 accelerator	US-PGPUB; USPAT	OR	ON	2006/06/19 11:11
S2	884	pipeline with accelerat$3	US-PGPUB; USPAT	OR	ON	2006/06/19 11:11
S3	220	pipeline near2 accelerat$3	US-PGPUB; USPAT	OR	ON	2006/10/03 13:45
S4	26	pipeline near2 accelerat$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/19 11:17
S5	0	accelerat$3 with load$3 with process$3 with external and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/19 11:17
S6	44	accelerat$3 with load$3 with process$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/20 08:19
S7	3	("5583964" "4956771" "5892962").pn.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:21
S8	10	mccarthy-paul.in.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:52
S9	1	"5619430".pn.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:53
S10	1	"6205400".pn.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:54
S11	8	"raw data" with (coprocessor co-processor) same (buffer queue FIFO)	US-PGPUB; USPAT	OR	ON	2006/06/20 10:56
S12	31	"raw data" with (coprocessor co-processor)	US-PGPUB; USPAT	OR	ON	2006/06/20 14:51
S13	171	"raw data" with (slave PE DSP)	US-PGPUB; USPAT	OR	ON	2006/06/20 14:51
S14	9	"raw data" with (slave PE DSP) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/20 14:54
S15	12	"processed data" with (coprocessor co-processor) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/20 14:54
S16	1	(US-6624819-$).did.	USPAT	OR	ON	2006/06/21 08:41

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S17	1	S16 and "160" with ("204" "206")	US-PGPUB; USPAT	OR	ON	2006/06/21 10:16
S18	165	output near2 queue with (address$2 pointer) near3 memory	US-PGPUB; USPAT	OR	ON	2006/06/21 10:22
S19	77	output near2 queue near5 (address$2 pointer) near2 memory	US-PGPUB; USPAT	OR	ON	2006/06/21 10:17
S20	19	output near2 queue near5 (address$2 pointer) near2 memory and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2006/06/21 10:17
S21	34	output near2 queue with (address$2 pointer) near3 memory and g06f$. ipc. not S20	US-PGPUB; USPAT	OR	ON	2006/06/21 11:06
S22	482	address near2 queue with (address$2 pointer) near3 memory and g06f$.ipc. not S20	US-PGPUB; USPAT	OR	ON	2006/06/21 10:22
S23	2	opcode near3 coprocessor with (send$3 transfer$4 transmit$4) with instruction	US-PGPUB; USPAT	OR	ON	2006/06/22 08:39
S30	1480	receiv$3 near3 data same tempora$4 near3 stor$3 same process$3 near3 data same (transmi$5 send$3 pass$3) near4 data	US-PGPUB; USPAT	OR	ON	2006/09/27 14:42
S31	538	(receiv$3 near3 data with tempora$4 near3 stor$3) same (process$3 near3 data) same ((transmi$5 send$3 pass$3) near3 data with process$3)	US-PGPUB; USPAT	OR	ON	2006/09/27 14:43
S32	5	(receiv$3 near3 data with tempora$4 near3 stor$3) same (process$3 near3 data) same ((transmi$5 send$3 pass$3) near3 data with process$3) same (pipeline accelerat$3)	US-PGPUB; USPAT	OR	ON	2006/09/27 14:45
S33	1	((data near3 tempora$4 near3 stor$3) with (prior before) near3 process$3) same ((transmi$5 send$3 pass$3) same (pipeline accelerat$3))	US-PGPUB; USPAT	OR	ON	2006/09/28 08:37
S34	84	((processor pipeline) with first near3 integrated adj circuit) and (memory DRAM) with (separate second) near3 integrated adj circuit	US-PGPUB; USPAT	OR	ON	2006/09/28 08:41
S35	177	((processor pipeline) with memory with separate near3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:42

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S36	38	((processor pipeline) with memory with separate near3 integrated adj circuit) same advantag$4	US-PGPUB; USPAT	OR	ON	2006/09/28 08:46
S37	3	((processor pipeline) with memory with separate near3 integrated adj circuit) same (faster speed failure)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:47
S38	0	((processor pipeline) with memory with separate near3 integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:47
S39	0	((processor pipeline) with memory with distinct near3 integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:47
S40	73	((processor pipeline) with memory with integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:51
S41	237	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/10/03 13:48
S42	41	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:54
S43	417	((processor pipeline) with memory with integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:54
S44	73	((processor pipeline) with memory with single near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:56
S45	1	((processor pipeline) with memory with (two multiple plurality) near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:25
S46	18	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (memory near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:27
S47	0	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (DRAM near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:27
S48	0	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (RAM near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:27
S49	130	((processor pipeline) near5 (first second) near2 chip) same ((RAM memory DRAM) near5 (first second) near2 chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:28

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S50	3	((processor pipeline) near5 (first second) near2 chip) same ((RAM memory DRAM) near5 (first second) near2 chip) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:29
S51	15	((processor pipeline) with (DRAM RAM memory) with separate near2 chip) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:39
S52	85	((processor pipeline) with (DRAM RAM memory) with (off-chip "off chip")) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:43
S53	21	((processor pipeline) with (DRAM RAM memory) with (off-chip "off chip")) with (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:41
S54	64	S52 not S53	US-PGPUB; USPAT	OR	ON	2006/09/28 10:12
S55	49	(memory DRAM RAM) with ("off chip" off-chip) with (cheap$2 expensive)	US-PGPUB; USPAT	OR	ON	2006/09/28 10:41
S56	0	("register file") with ("off chip" off-chip) with (cheap$2 expensive)	US-PGPUB; USPAT	OR	ON	2006/09/28 10:42
S57	86	("register file") with ("off chip" off-chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 10:43
S58	48	("register file") near3 ("off chip" off-chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 11:04
S59	199	((coprocessor accelerator DSP PE assist) with (read$3 receiv$3) with data with (buffer memory) with processor) same (process$3 near3 data) same (writ$3 send$3 transmit$4) with data with (buffer memory)	US-PGPUB; USPAT	OR	ON	2006/09/28 11:07
S60	22	((coprocessor accelerator DSP PE assist) with (read$3 receiv$3) with data with (buffer memory) with processor) same (process$3 near3 data) same (writ$3 send$3 transmit$4) with data with (buffer memory) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/28 11:59
S61	27742	buffer with ("integrated circuit" chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 11:59
S62	6	buffer near3 separate near3 ("integrated circuit" chip) with (processor pipeline)	US-PGPUB; USPAT	OR	ON	2006/09/29 11:20
S63	34	buffer near3 ((separate near3 ("integrated circuit" chip)) (off-chip "off chip")) with (processor pipeline)	US-PGPUB; USPAT	OR	ON	2006/09/28 12:01

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S64	44	buffer near3 ((separate near3 ("integrated circuit" chip)) (off-chip "off chip")) with (processor pipeline CPU)	US-PGPUB; USPAT	OR	ON	2006/09/29 08:11
S65	1	"6205400".pn.	US-PGPUB; USPAT	OR	ON	2006/09/29 08:11
S66	7	("2" two) near2 stage near3 (multiplier multiply multiplication) with latch	US-PGPUB; USPAT	OR	ON	2006/09/29 11:23
S67	38	multiply adj accumulate with latch	US-PGPUB; USPAT	OR	ON	2006/09/29 11:28
S68	0	coprocessor same multiply adj accumulate with latch	US-PGPUB; USPAT	OR	ON	2006/09/29 11:28
S69	47	coprocessor with multipl$7 adj accumulat$3	US-PGPUB; USPAT	OR	ON	2006/09/29 13:10
S70	276	pointer with data with "input buffer"	US-PGPUB; USPAT	OR	ON	2006/09/29 13:10
S71	38	pointer with next with data with "input buffer"	US-PGPUB; USPAT	OR	ON	2006/09/29 13:12
S72	7	read adj pointer with "input buffer" and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:14
S73	20	pointer with "input buffer" and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:16
S74	3	pointer with buffer with input with (execution functional) near2 unit and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:18
S75	43	pointer with buffer with input with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:19
S76	151	pointer with buffer with (operand data) with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:19
S77	29	pointer with buffer with operand with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:22
S78	125	read near3 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:23
S79	112	read near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:24
S80	24	queue near3 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:34
S81	13	queue near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:35
S82	25	(queue fifo) near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:38
S83	5	stor$3 near5 buffer near2 pointer near5 queue and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 15:43

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S84	14	processor with coprocessor with separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2006/09/29 16:26
S85	109	"front end" with separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2006/09/29 16:27
S86	61	"front end" near3 separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2006/09/29 16:27
S87	0	"front end" near3 separate near3 (chip "integrated circuit") and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 16:27
S88	4	"front end" with separate near3 (chip "integrated circuit") and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 09:34
S89	3	coprocessor with execut$3 with (division divide) near3 (operation instruction) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 12:36
S90	319	712/34.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:02
S91	250	712/35.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:03
S92	405	712/200.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:04
S93	595	712/225.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:08
S94	1	"6282627".pn.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:08